PATENT **ALBRP228US**

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Date: October 6, 2008 /Rebecca Stanford/
Rebecca Stanford

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Mark Flood, *et al.*

Serial No: 09/862,941

Filing Date: May 22, 2001

Examiner: Kyung H. Shin

Art Unit: 2143

Title: APPARATUS FOR MULTI-CHASSIS CONFIGURABLE TIME SYNCHRONIZATION

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
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REPLY BRIEF

Dear Sir:

Appellants' representative submits this Reply Brief in response to the Examiner's Answer mailed August 6, 2008. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP228US].

REMARKS

As indicated at page 3 of the Examiner's Answer (dated August 6, 2008, hereinafter referred to as "EA"), claims 1 and 3-53 (rather than claims 1-53) are currently pending and are presently under consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein. In particular, the following comments address deficiencies contended in the Examiner's Answer to appellants' Appeal Brief.

I. Rejection of Claim 1 Under 35 U.S.C. §112, First Paragraph

Claim 1 stands rejected under 35 U.S.C. §112 as failing to comply with the written description requirement. Withdrawal of this rejection is respectfully requested for at least the following reasons. The specification discloses in full, clear, concise, and exact terms that which can enable any person of ordinary skill to carry out the claimed subject matter.

At pages 3 and 4 of EA, it is contended that there is no disclosure within the specification or original claims for a time synchronization apparatus that "is configurable to operate as both a synchronization master and a synchronization slave" as recited in independent claim 1. Foremost, this rejection was formerly asserted in the Final Office Action (dated December 27, 2007), but was subsequently withdrawn in view of persuasive comments. (*See* Advisory Action dated March 19, 2008 at pg 3, "The 112 rejection has been withdrawn because of persuasive arguments in remarks."). Regardless, it is readily apparent that support for these features is disclosed in numerous portions of the specification. "For example, the Synchlink circuit or chip 314 is configurable by the host processor 302 to operate the synchronization module 300 as ***a synchronization master or a synchronization slave***." (*See* pg. 37, ll. 9-11; *see* also pg. 17, ll. 1-10). Clearly, there is support for a single component (*e.g.*, the synchronization apparatus) that is configurable to operate as a master, and also configurable to operate as a slave. Therefore, it is illogical to suggest that this component cannot be configurable to operate as both.

The Examiner freely admits that there is support for the apparatus to act as either a master or a slave, but tacitly ignores that if the claim language actually recited "an

apparatus that is configurable as either a master or a slave" then a hypothetical prior art reference that taught an apparatus that is configurable as a master (but not a slave) or a slave (but not a master) would still read on the claim, even though the prior art only teaches a single configurable state while applicants' specification (and the claimed subject matter) clearly recites that the apparatus can be configurable as both. Applicants have adequate disclosure for such and have selected to narrow the scope of the claim to suitably prevent such broad interpretation. It is unconditionally illogical to accept that the apparatus can be configurable as a master and also configurable as a slave (as the Examiner concedes), but then reject that the apparatus can be configured as both.

If, as the Examiner maintains, there is no support for the apparatus to be configurable as both a master and a slave, then the Examiner must allege that one of the two is not supported—otherwise, there is *de facto* support for "both." Yet, the Examiner has failed to show that the apparatus is not configurable as a master (in fact, the Examiner admits there is support for this), and further the Examiner admits there is support for configurability as a slave. Thus, there is support for a single apparatus that can do ***both***.

In fact, the Examiner is not here rejecting what is claimed, but rather is rejecting elements that are **not** claimed. The sole basis for this rejection is the Examiner's position that there is no support for the apparatus to be configurable as both ***at the same time***. Without the "at the same time" clause, the Examiner's argument is self-refuting, yet such limitations are not found in the claim. That is, the claim does ***not*** recite "at the same time" and it is not clear what evidence the Examiner employs to determine the *ad hoc* addition of such limitations to the claim represents a reasonable interpretation of the claim.

Pointedly, it is impermissible for the Examiner to insert arbitrary limitations into the claim, and then argue appeallants have not supported in their disclosure those arbitrary limitations invented by the Examiner. Yet, this is precisely what was done here. Accordingly, this rejection should be reversed.

Furthermore, although appellant's representatives believe it is irrelevant since proper analysis should not get so far (since the claims do not recite "at the same time"), it should be noted that there is in fact support in the specification for operating as both a master and a slave substantially simultaneously. For example, the synchronization

apparatus can act as a local master, yet at the same time act as a global slave. (*See* pg. 17, ll. 1-11).

II. Rejection of Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 Under 35 U.S.C. §103(a)

Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, *et al*. (US 4,807,259, hereinafter referred to as "Yamanaka") in view of Voth (US 6,199,169). It is respectfully submitted that this rejection should be reversed for at least the following reasons. Neither Yamanaka nor Voth, either alone or when combined, disclose all the claimed features. Moreover, Yamanaka and Voth produce an inoperative combination and/or do not yield a reasonable expectation of success to make the proposed combination. Therefore, these references are not permissibly combinable, and furthermore, the Examiner relies upon mere conclusory statements to uphold these rejections.

At page 32 of EA, it is noted that Voth was found to be materially deficient to disclose the claimed synchronization apparatus, in a Decision on Appeal (February 9, 2007), by the Board of Patent Appeals and Interferences (BPAI). Accordingly, the BPAI reversed all rejections maintained by the Examiner, but provided new grounds for rejection under 37 C.F.R. 41.50(b) for claim 1 alone (*e.g.*, Yamanaka). Accordingly, while the Examiner quotes the board: "we did not review claims 2-52 to the extent necessary to determine whether these claims are patentable over the Voth patent or other cited references," the result of this decision was therefore that claims 2-52 had no rejections outstanding. Accordingly, features included in canceled claim 2, which are not disclosed or suggested by the additional references cited by the BPAI have been incorporated into the independent claims. Therefore, it is believed that all claims are allowable over the cited art.

In response to the arguments at page 33, appellants' representatives' primary purpose of mentioning technological advances was to refute the Examiner's assumption that Voth could be applied to the Internet at large given certain "technological advances," and therefore certain other claimed features were argued to be obvious by applying Voth to the Internet. However, this is not possible, even assuming the express "tick" value

recited in Voth of 10 μs (*see* col. 8, ll. 60-61). This means that the round-trip travel time between two nodes must be about ½ a tick or 5 μs or else (the appearance of) synchronization will not be achieved and the SYNC message will be rejected (*see* col. 8, ll. 44-46), with the exemplary round trip travel time being about 1 μs (*see* col. 8, ll. 55-56). Under these conditions, it is evident that, because all SYNC messages must have a round-trip travel time of no more than 1 μs, Voth cannot be applied to the Internet at large. Conversely, increasing this 1 μs threshold would serve to make the method of Voth increasingly ineffectual for synchronization since the accuracy of synchronization is a function of the round-trip travel time (*see* col. 8, ll. 46-49). This is so because propagation delay is ignored by the method, however, by ignoring propagation delay, delays greater than an upper threshold (*e.g.*, 1 μs) must be rejected or the synchronization will be too inaccurate. The Examiner indicated that technological advances could make it possible to apply Voth's method to the Internet, so appellants' representatives responded by illustrating that even at the speed of light, the theoretical limit of network communication no matter how technologically advanced and with no interference or traffic, Voth cannot be applied to the Internet.

The Examiner notes that the "tick" of Voth is not the same thing as processor speed. While an accurate statement, it is inaccurate to suggest that "*this 'tick' has no relation to the clock speed*," when in fact the two are highly correlated. A 'tick' is the duration of one tick of the system timer interrupt, and does in fact depend upon the clock interrupt frequency of the particular hardware platform because it is optimal to make this equal to or a multiple of the clock speed of the processor. Hence, clock speed, has historically been an accurate proxy for a tick, even though as the Examiner notes these are not exactly the same. However, regardless, the salient point is this: Voth's contribution to the field is a time synchronization method that works by treating round-trip latency as zero. While novel at the time, this method understandably limits its applications to only those situations in which latency is low enough to be negligible. That is, the latency must be lower than the detectable precision of the clock, which is not realistic for anything but highly specialized, high-speed networks. Either *via* new technology or some other reason, raising the value of the "tick" serves to make the synchronization less accurate, while lowering the "tick" value reduces the spatial range

over which the method can be applied under even the most optimal conditions possible (much less real-world network environments) due to the inherent limitations of the speed of light. Moreover, this spatial range parameter is a very real factor in the usefulness of Voth's method, and certainly precludes application to the Internet at large, which was suggested by the Examiner to support various claim rejections.

At page 34, it is disputed that Voth treats latency as zero in order to accomplish synchronization. This argument is clearly erroneous, as Voth, to effectuate synchronization, subtracts the first time stamp of the master from that of the slave ***with no offset for the travel time*** of the SYNC message between the two nodes (see col. 6, ll. 60-63). Moreover, Voth further indicates that when the above calculation results in a negative number, then the slave is considered lagging and is adjusted by the difference (*see* col. 6, line 63 – col. 7, line 2). If the subtraction is greater than or equal to zero, then the second master time stamp is employed such that the slave stamp is subtracted from the second master stamp (as opposed to the first master being subtracted from the slave time stamp which yields in that case a positive number). If this value is zero, then the clocks are already synchronized, but if it is negative, then the slave leads and is adjusted by the difference between the time stamps, and that alone (*see* col. 7, ll. 3-14).

This means that the amount of adjustment for lagging slave clocks is determined by SYNC messages transmitted ***from*** *the master* (even though the actual latency for such traffic is not accounted for), while the adjustment for leading slave clocks (or when already in synch) is determined by SYNC messages transmitted ***to*** *the master* (but again the actual amount of latency is not accounted for). Or, as the reference states, the method is not dependent upon the assumption that transmission delay to a node is the same as that from the node (see col. 7, ll. 14-18). In fact, Voth treats the transmission delay as zero in both cases, so it does not matter if speed might vary according to direction as long as the round-trip delay is less than what can be distinguished by the clock (*i.e.*, ½ a tick). Appreciably, the master records a time stamp, transmits it to the slave, which also records a time stamp, and then sends it back to the master for the third time stamp. Strict comparisons in time stamps are made to determine the appropriate adjustment, meaning each one-way travel time value is not accounted for, and thus assumed to be negligible. If travel time where accounted for, then Voth would have to appreciate that merely

relying upon the sign of the time stamp difference would lead in many cases to an incorrect reading as to whether or not the slave clock lagged. For example, if the slave clock lags the master clock by 1 second, but the travel time is 2 seconds, then looking at the time stamps alone (as Voth teaches) would lead to the false assumption that the slave clock actually leads the master by 1 second, when it does in fact lag by 1 second. It is readily apparent that Voth does not include transmission delay in any synchronization adjustment and does not even disclose a mechanism for detecting one-way latency (but rather only total round-trip latency which is compared to the accuracy threshold to determine if the message is rejected or not). It is for this reason that Voth does not provide true synchronization, but rather the "appearance of synchronization" (*see* col. 8, ll. 66-67), as true synchronization would require accounting for one-way latency. Therefore, transmission delay is treated as zero but round trip latency is bounded by an upper limit based upon clock sensitivity/precision, which is why virtually instantaneous network speeds are required for a successful implementation of Voth's method, and also why the application of Voth's method is so limited in scope.

At page 35, it is argued "*Voth states that a message will be rejected if the round trip time exceeds a predefined threshold. There is no mention that 1/2 clock tick is the indicated citation.*" In response, appellants' representatives note that Voth indicates that this "predefined threshold" is in fact 1/2 a tick, wherein a tick is defined as 10 μs. Accordingly, this "predefined threshold" must be no greater than 5 μs, or the "appearance of being synchronized" (*i.e.*, Voth's method) cannot be achieved. (*See* col. 8, ll. 44-67).

In addition, it is further argued that Voth teaches transmitting message frames at a fixed period of about 50 μs as recited by dependent claim 4. This argument is based upon the fact that Voth teaches a fixed period of 20 second. Appellants' do not dispute that every 20 seconds constitutes a fixed period. What is disputed is that a fixed period ***of 20 seconds*** teaches or suggests a fixed period ***of 50 μs***. The fixed period feature is recited in claim 3, but claim 4 further limits claim 3 to a period of about 50 μs. This further limitation should not be ignored, yet the rejection analysis does just that, treating claim 4 as though "50 μs" is not recited. Further still, this value is about 400,000 times shorter in duration than the fixed period of Voth, and, moreover, the update time in Voth requires 4 seconds to complete, so it would be illogical to suggest that Voth renders these features

obvious when such a notion would entail 80,000 update requests being transmitted before a single update is completed.

XII. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited reference. Accordingly, it is respectfully requested that the Examiner's rejections be reversed.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Respectfully submitted,

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